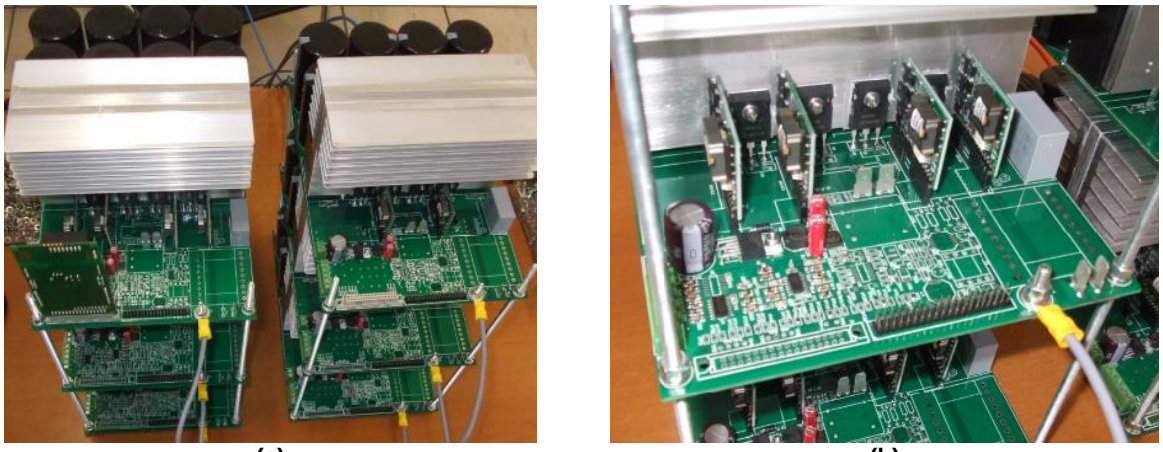
Gate drivers and Resonant AC-Link power supplies

In order to provide accurate response to the important questions rose by designers, two power systems were designed respectively in Three-level and in Two-level topologies.

Design of a Three-Level T-type inverter was completed within the cooperation between Infineon Technologies Austria A.G. and the Design House TF S.r.l. This specific design was studied in order to allow easy replacement of different discrete devices and easy handling of the different parts of the system. The power stage shows extremely low parasitic inductance: below 35nH.

Special attention in this design was dedicated to the reduction of the E.M.I. level, both in common mode and in differential mode. Gate driver design, using Infineon´s 1ED compact gate drivers, allow reaching over 50kV/µs, and the auxiliary power supply, which uses an original resonant AC-link design with local transformer with reduced coupling capacitances and improved insulation level over 5kV_{ac}, permits reaching high dv/dt immunity level.



(a) (b)

Figure 1: (a) Three-Level Three-phase T-Type system. Assembly phase of two Three-phase systems and (b) close up view of the single phase structure before assembling the EMI filters.

In Table 1 the most important technical parameters of the T-Type design are listed.

Table 1: Main electrical characteristic of the Three-Level T-Type Testing System

Characteristic	Value/Description	Unit
Semiconductor packages	Discretes IGBT and SiC-MOSFET in TO-247, 1 per switch, 4 per phase, 12 in total	
Semiconductor types	S5 IGBT, Rapid diodes, SiC Gen. 5, SiC-MOSFET	
Input DC Voltage	500…800	V_{DC}
Output AC Voltage	400 (230 in single phase)	V_{ac}
Thermal resistance $R_{th\text{-}ca}$	1,05	K/W
Output current	35	$I_{(RMS)}$
Nominal output power	21 (7 per phase)	kW
Maximum P_{out} per 10s	30	kW
Maximum output current	30	$I_{(RMS)}$
Max allowable dv/dt	50	kV/µs
Max allowable di/dt	5	A/ns
Insulation voltage	5 per 60s	kV_{ac}
Stray inductance L_σ	35	nH
Max case Temp. $T_{c(max)}$	120	°C
Coupling capacitance C_p	1200 overall including output filters	pF

In Figure 3 it is depicted a generic block diagram of the entire Three-Level T-Type Inverter system. This is referred to a single-phase output stage and it is exploded in a three-phase unit. Gate driver it is also represented in detail. In the red rectangles are indicated respectively the Coreless Transformer gate drivers and the floating power supply, provided by small additional local H.F. transformer. This transformer provides additional insulation, up to 5kV$_{ac}$ together to a strong reduction of the coupling capacitance. Both these solutions provide excellent dynamic response and voltage stability at very high switching frequency and extremely high dv/dt levels, approaching 50V/ns.

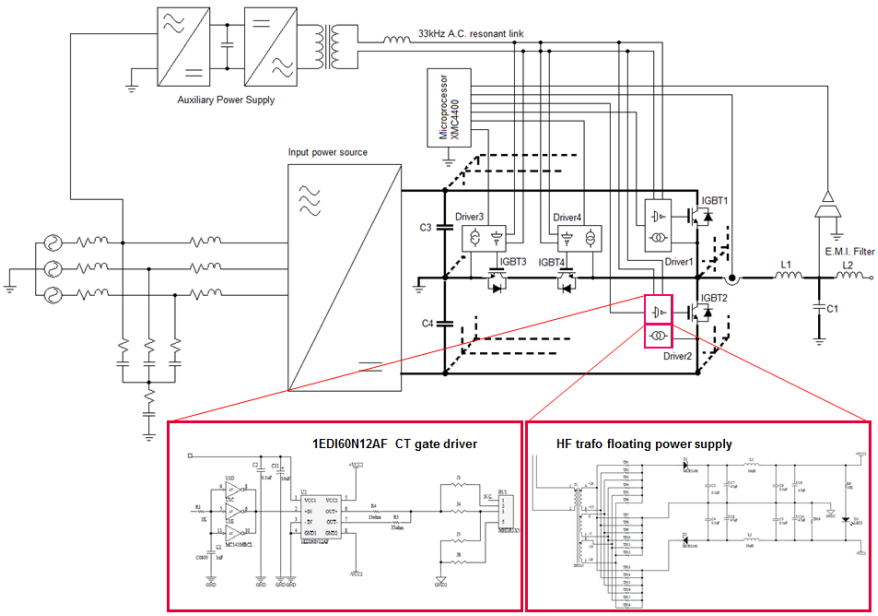


Figure 2: Block diagram of the Three-Level T-Type Inverter system. It is represented for a single-phase system and it is exploded in a three-phase stage. Details of the coreless transformer and HF isolation transformer used are indicated in the red rectangles.

The other subsystems, part of the Three-Level T-Type solution, are listed with a short description of the device used in Table 2.

Table 2: Details of the subsystem of the Three-Level T-Type solution

Subsystems	General Description	Details of the device used
Main passive components	DC-Link capacitors	1mF/800V – 0,5mF/1600V Electrolytic 105°C 1360mA(RMS) 2x40µF/900V Film capacitor
	Output Chokes	L1=1mH (Fe-Si E-Cores, Litz-wire), 4kVac insulation
	EMI Filter	Details at chapter 2.2
Driver stage	Separated daughter boards with Coreless Tans former	1EDI60N12AF and selectable positive/negative VGE
Microprocessor	XMC4400 drive card KIT	XMC4400
Auxiliary Power Supply	Resonant AC Link	Pout=25W, VISO=5kVac, Cp=12pF

Two level inverter design

Design of the Two-level inverter was also completed within the cooperation between Infineon Technologies Austria and TF S.r.l. This system was designed to meet the SiC-MOSFET requirements, although using standard PCB material and classic passive components. In this case, special care was dedicated to the dv/dt immunity and insulation levels, in order to

reach the highest possible dv/dt without impacting on the reliability and on the system stability. Further details of the designed power stage are shown in Fig. 4 and indicated in Table 3. The block diagram is reported in Fig. 5.

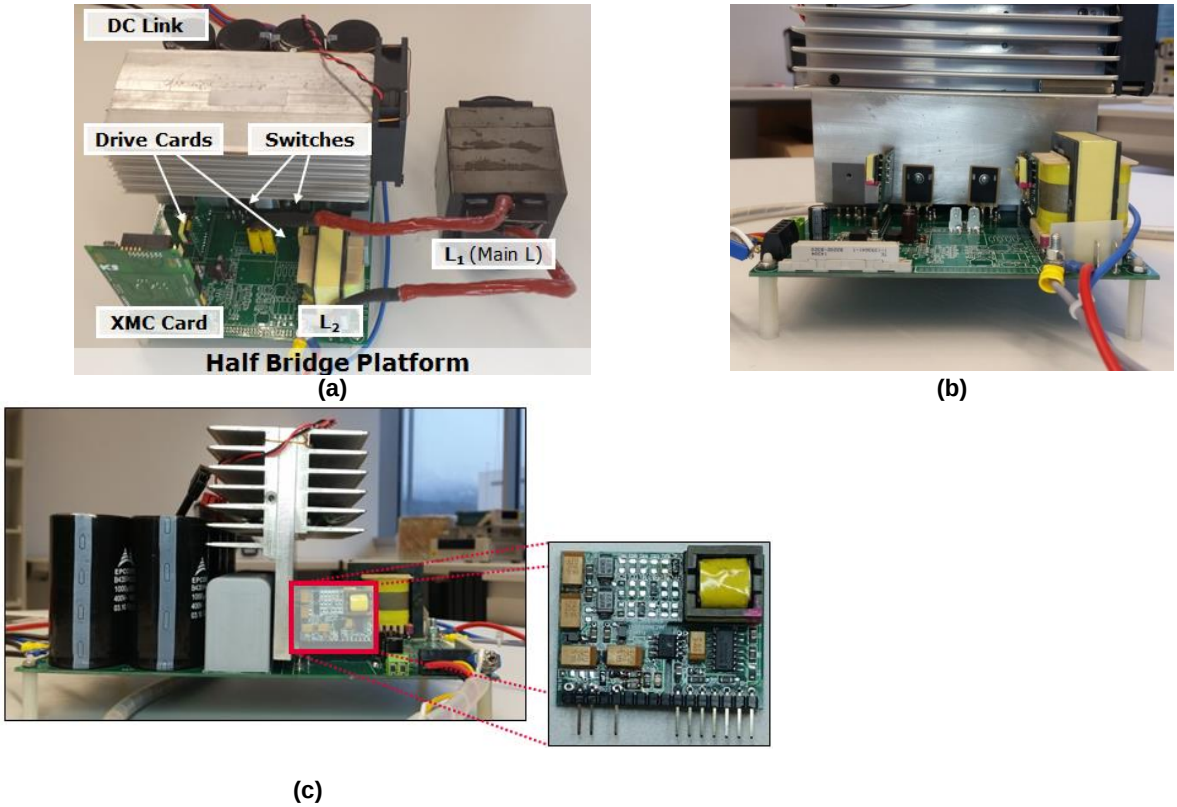


Figure 3: (a) close up view of a single-phase unit with short description of the main subsystems, (b) front view of the single-phase unit, (c) side view of the single-phase unit with a close-up view of a gate driver daughter board.

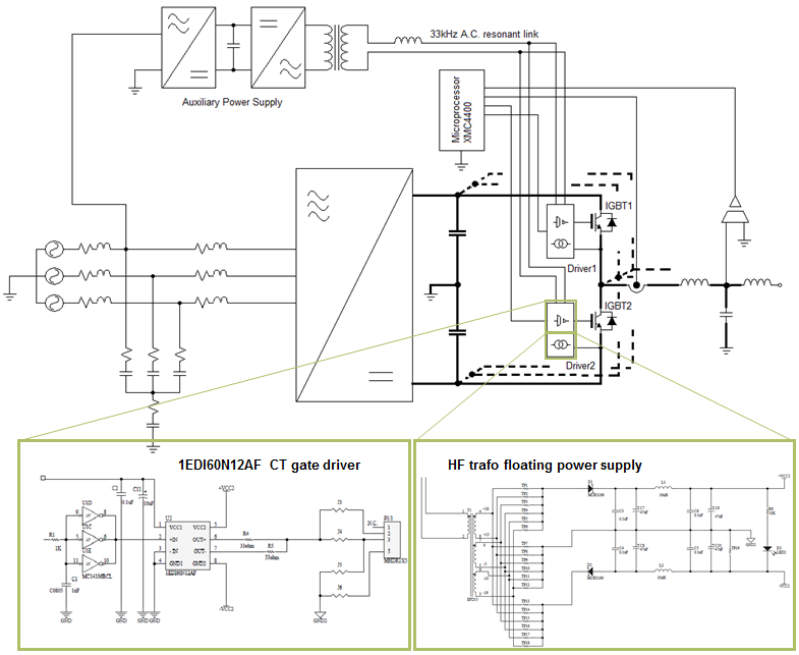


Figure 4: Block diagram of the Two-Level Inverter system. Block diagram is shown for a single-phase system and it is exploded in a three-phase unit. Details of the coreless transformer and HF isolation transformer are indicated in the green rectangles.

Table 3: Main electrical characteristic of the Two-Level Testing System

Characteristic	Value	Unit
Semiconductor packages	Discrete IGBT and SiC-MOSFET in TO-247-3 and in TO-247-4, 1 discrete device per switch, 6 in total (possibility for paralleling operation of 2 x TO-247-3 and 2 x TO-247-4 per switch)	
Semiconductor types	S5/H5 IGBT, SiC MOSFET, SiC Gen5/Rapid diode	
Input DC Voltage	500…700	V_{DC}
Output AC Voltage	400 (230 in single phase)	V_{ac}
Thermal resistance $R_{th\text{-}ca}$	1,05	K/W
Output current	30	$I_{(RMS)}$
Nominal output power	18 (6 per phase)	kW
Maximum P_{out} per 10s	25	kW
Maximum output current	25	$I_{(RMS)}$
Max allowable dv/dt	50	kV/µs
Max allowable di/dt	5	A/ns
Insulation voltage	5	kV_{ac}
L_σ	34	nH
$T_{c(max)}$	120	°C
C_p	1100	pF