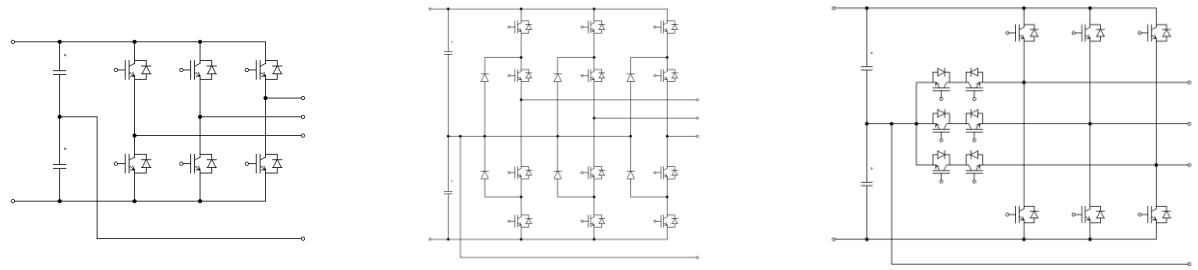
Hybrid SiC/Si solutions in Photovoltaic (PV) and UPS

Introduction

In today's PV, UPS and GPI systems, three-level output inverters are a common design solution giving an excellent cost/performance ratio. The technical advantage over the classical two-level B6 inverter represented in figure 1 (a) is a reduction of switching losses and filtering effort, at the expenses of higher circuit complexity. Two commonly found three-level inverter designs in the low to mid power range are the *Neutral Point Clamping Diode*, thereinafter NPC-1 or I-Type, illustrated in Figure 1 (b) and *Neutral Point Clamping Transistor*, thereinafter NPC-2 or T-Type, in Figure 1 (c).



(a) **(b)** **(c)**

Figure 1: most commonly used Inverter configurations: (a) two-level (B6, Six-Pack) Inverter; (b) three-level Neutral Point Clamping Diodes (NPC-1) Inverter; (c) three-level transistor clamped (T-Type) Inverter;

It is demonstrated that it is convenient to use of the T-Type inverter at switching frequencies typically lower than 30…35 kHz because of the lower conduction losses. On the contrary, NPC-1 topology becomes more competitive at higher frequencies. With the emerging SiC semiconductor technology the degrees of freedom for the designer become higher, opening the path to new scenarios. Fast 1200V SiC switches make T-Type inverters attractive for higher frequencies. According to the multi-objective optimization performed in [6], even the transition back to a two-level solution can be considered because CoolSiC™ technology can achieve higher efficiency and reduce the bill of materials.

In this paper, the potential of CoolSiC™ MOSFETs in two-level B6 as well as three-level T-Type inverters is investigated experimentally. Measured system efficiencies together with loss-breakdown estimations demonstrate the advantages and disadvantages of the different Si, SiC and hybrid SiC/Si solutions.

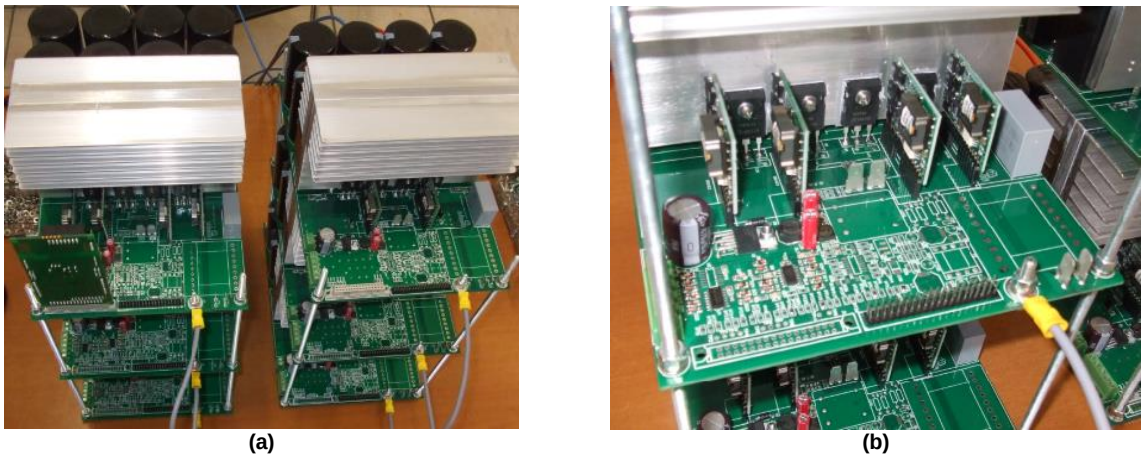
Description of the power systems in testing and the test set up

To provide accurate response to the important questions risen by designers and mentioned in the introduction of this paper, two power systems were designed, respectively in three-level and in two-level topologies.

T-Type three-level inverter design

Designing a three-level T-Type inverter was completed within the cooperation between Infineon Technologies Austria A.G. and Infineon's Design House T.F. S.r.l. This specific design, as illustrated in Figure 2, was created to allow simple replacement of different discrete devices and easy handling of the different parts of the system. The power stage features a parasitic inductance below 35 nH, including the stray inductance of the discrete packages.

Special attention in this design was dedicated to the reduction of the EMI level, both in common mode and in differential mode. Gate driver design, using Infineon´s 1ED60N12AF compact gate drivers, allows reaching over 50 kV/µs. Auxiliary power supply, which uses an original resonant AC-link design with local HF transformer, reduced coupling capacitances and improved insulation levels to exceed 5 kV_{AC}. It permits reaching high dv/dt immunity levels.



(a) (b)

Figure 2: (a) Three-level three-phase T-Type system. Assembly phase of two three-phase systems and (b) close up view to the single-phase structure prior to assembling the EMI filters.

In Table 1 the most important technical parameters of the T-Type design are listed.

Table 1: Main electrical characteristic of the three-level T-Type testing system

Characteristic	Value/Description	Unit
Semiconductor packages	Discrete IGBT and CoolSiC™ MOSFET in TO-247, 1 per switch, 4 per phase, 12 in total	
Semiconductor types	S5 IGBT, Rapid diodes, SiC Gen. 5, CoolSiC™ MOSFET	
Input DC Voltage	500…800	V_{DC}
Output AC Voltage	400 (230 in single phase)	V_{AC}
Thermal resistance $R_{th\text{-}ca}$	1,05 (TO-247 case to ambient)	K/W
Output current	35	A_{RMS}
Nominal output power	21 (7 per phase)	kW
Maximum P_{out} per 10s	30	kW
Maximum output current	30	A_{RMS}
Max allowable dv/dt	50	kV/µs
Max allowable di/dt	5	kA/µs
Insulation voltage 1 min	5	kV_{AC}
Stray inductance L_σ	35	nH
Max case Temp. $T_{c(max)}$	120	°C

Figure 3 depicts a generic block diagram of the entire three-level T-Type inverter system. This refers to a single-phase output stage. The gate driver is also represented in detail. In the highlighted rectangles in Figure 3, the Coreless Transformer gate drivers and the floating power supply based on HF-Transformer are indicated. This additional HF-Transformer provides further insulation up to 5 kV_{AC} combined with a reduction of the auxiliary power supply parasitic capacitance. Both these solutions provide excellent dynamic response and voltage stability at very high switching frequencies and extremely high dv/dt levels, approaching 50 kV/µs.

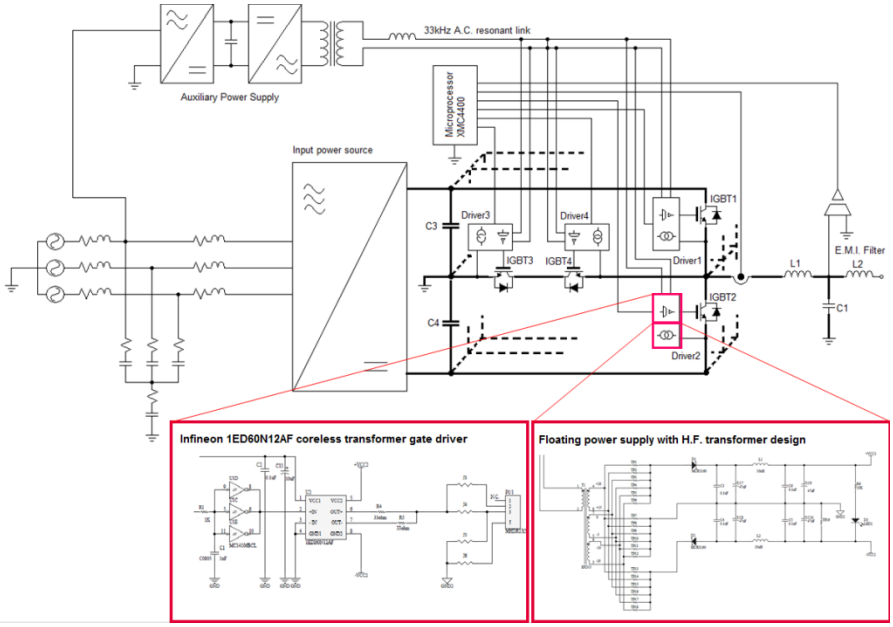


Figure 3 : Block diagram of the three-level T-Type inverter system. It is represented for a single-phase system. Details of the coreless transformer drivers and HF transformer are highlighted in the rectangles.

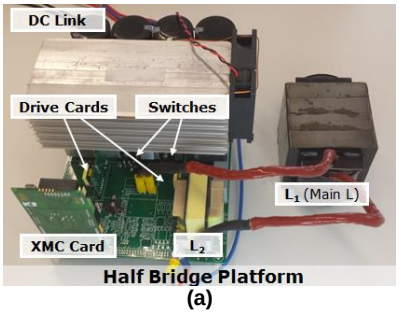
The other subsystems that are part of the three-level NPC-1 inverter are listed, with a short description of the device used, in Table 2.

Table 2: Details of the subsystem of the three-level T-Type solution

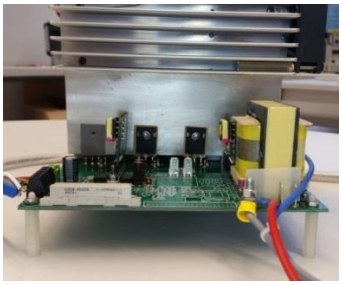
Subsystems	General Description	Details of the device used
Main passive components	DC-Link capacitors	1mF/800V – 0,5mF/1600V Electrolytic 105°C 1360mA$_{RMS}$ 2×40µF/900V Film capacitor
	Output Chokes	L_1=1mH Fe-Si E-Cores, Litz-wire, 4kV$_{AC}$ insulation
	EMI Filter	Details at chapter 2.2
Driver stage	Separated daughter boards with Coreless Transformer driver	1EDI60N12AF and selectable positive/negative gate voltage
Microprocessor	XMC4400 drive card KIT	XMC4400
Auxiliary Power Supply	Resonant AC Link	P_{out}=25W, V_{ISO}=5kV$_{AC}$, C_p=12pF

Two-level inverter design

The design of the two-level inverter was also completed within the cooperation between Infineon Technologies Austria A.G. and T.F. S.r.l. This system was designed to meet the CoolSiC™ MOSFET requirements, despite using standard PCB material and classical passive components. In this case, special care was dedicated to the dv/dt immunity and insulation levels to reach the highest possible dv/dt without negative impact on the reliability and on the system's stability. Further details of the power stage designed are represented in Figure 4 and indicated in Table 3. The block diagram is reported in Figure 5.



(a)



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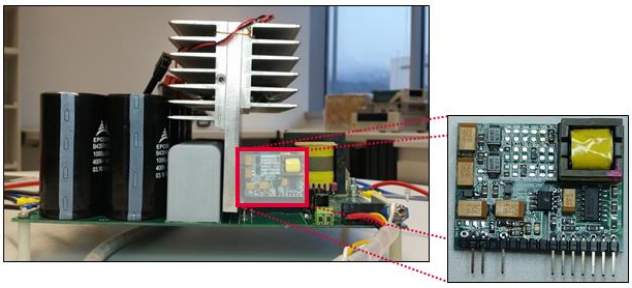


(c)

Figure 4: (a) close up view of a single-phase unit with short description of the main subsystems, (b) front view of the single-phase unit, (c) side view of the single-phase unit with a close-up view of a gate driver daughter board.

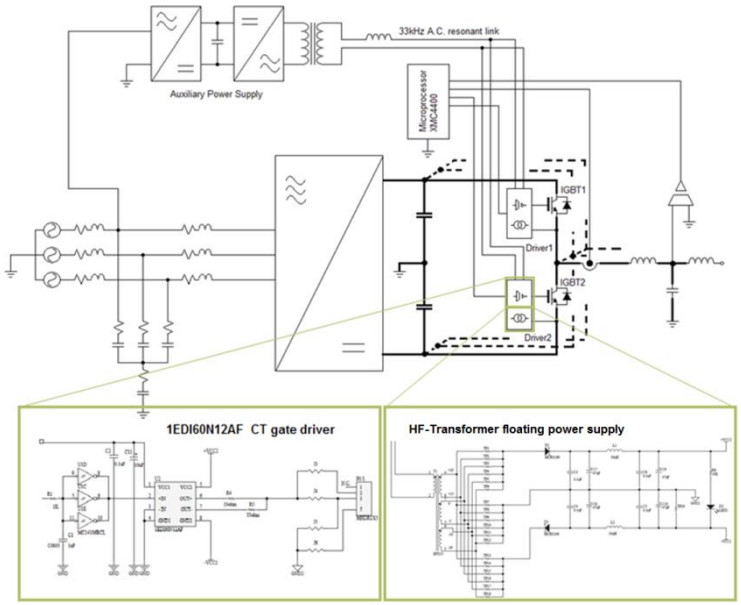


Figure 5: Block diagram of the two-level inverter system, sketched for a single-phase. Details of the coreless transformer and HF isolation transformer are indicated in the highlighted rectangles.

Table 3: Main electrical characteristic of the two-level testing system

Characteristic	Value	Unit
Semiconductor packages	Discrete IGBT and CoolSiC™ MOSFET in TO-247-3 and in TO-247-4, 1 discrete device per switch, 6 in total (possibility for paralleling operation of 2 x TO-247-3 and 2 x TO-247-4 per switch)	
Semiconductor types	S5/H5 IGBT, CoolSiC™ MOSFET, SiC Gen5/Rapid diode	
Input DC Voltage	500…700	V_{DC}
Output AC Voltage	400 (230 in single phase)	V_{AC}
Output current	30	A_{RMS}
Nominal output power	18 (6 per phase)	kW
Maximum P_{out} per 10s	25	kW
Maximum output current	25	A_{RMS}
Max allowable dv/dt	50	kV/µs
Max allowable di/dt	5	kA/µs
Insulation voltage	5	kV_{AC}
L_σ	34	nH
$T_{c(max)}$	120	°C

L-C-L output filter

The architecture of the output filter was designed using a classical L_1-C_1-L_2 configuration, as illustrated in Figure 6. L_1 is the output filter, C_1 is the output voltage filter and L_2 is the output EMI part of the filter. L_1 was dimensioned to allow a total ripple of 2 A_{pk}. This results in an inductor of 1 mH ±10% featuring

Fe-Si E-Cores. The inductor is Class H designed for switching frequencies up to 50 kHz and DC-currents of up to 30 A in continuous operation at 150 °C. Equivalent series resistance amounts to R_{ESR}=25 mΩ and parasitic capacitance achieved is C_p=280 pF. C_1 is a 3.3 µF 2 kV_{AC} film capacitor. L_2 is a 100 µH Fe-Si E-Core inductor.

Figure 6: L-C-L output and EMI filter (a) single-phase schematic and (b) three-phase configuration. (c) L_1 inductor appearance and (d) output filter C_1-L_2 assembled on the PCB board.

Test set-up and procedure

The test and measurement setup including all laboratory equipment is detailed in Figure 7.

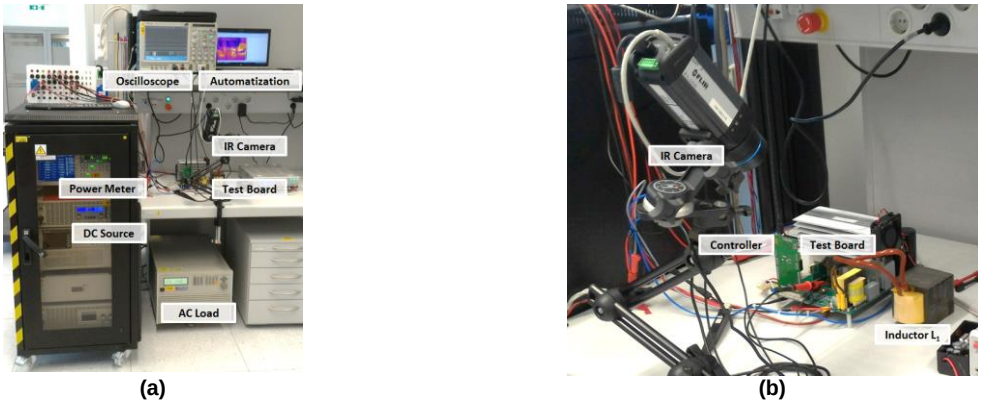


Figure 7: Fully automated test setup (a) including all laboratory equipment and (b) board close-up view

The test procedure was fully automated to ensure reproducibility and fair comparison, especially regarding thermal behavior. Table 4 provides an overview of the test conditions and procedure.

Table 4: Test conditions and procedure

Parameter	Value
Constant input voltage	700…750 V_{DC}
Constant Modulation factor	> 90% depending on the test case, topology and frequency
Output voltage	230 V_{AC} ±10 V_{AC}
Third Harmonic Injection	No
Output current (power)	1.5 A_{RMS} … 24 A_{RMS} (0.35 kW…5.5 kW)
Output current variation	Output current is increased in steps of 1.5 A_{RMS} every 300 seconds
End condition	I_{out}=24 A_{RMS} or package case temperature of 100°C is reached

The criteria defined for the test series are listed in Table 5 and basically determine the R_G selection and thus the switching speed. The goal is to maximize switching speed to keep high efficiency and lowering device temperatures. However, as boundary conditions, SOA and EMI/RF limits have to be met.

Table 5 Test criteria – safety and EMI limits.

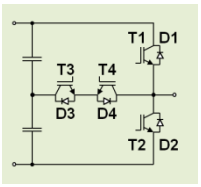
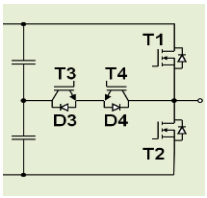
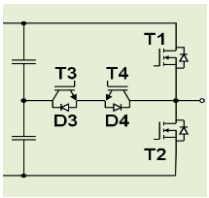
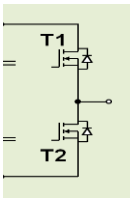
Test Cirteria and test conditions
V_{CE} ≤ 80% $V_{(BR)CEs}$ at turn-off
V_{AK} ≤ 80% V_{rrm} at turn-on
V_{GE} within data sheet specifications
dv/dt at turn-on and dv/dt at turn-off < 50 kV/µs

Test results

In this section, the performance of a three-level T-Type inverter with a combination of 1200 V and 600/650 V IGBTs is evaluated and compared to pure SiC and hybrid SiC/Si alternatives. To limit the degrees of freedom, there was no chip size variation for a given device during measurements. The selection of the 1200 V devices is based on the DC current rating given in the correlating data sheet. Fast switches were chosen for these positions. 650 V switches were always the same throughout all tests as S5 IGBTs lead to the best trade-off related to conduction and switching losses for this application. Regarding the diode, fast Si diodes as well as SiC Schottky Barrier Diodes (SBD) were selected. Both devices share the same DC current rating at 100 °C case temperature.

Table 6 provides a summary of these performance comparisons. For each scenario the circuit, the devices under test, the switching frequency f_{sw} as well as the maximum achievable output power P_{max} and efficiency η_{max} are given. The plot of the efficiency versus system output power is depicted in **Figure** 8. The power loss distribution of the different components within the systems is summarized in Figure 9.

Table 6 Test scenarios and results:

	3L-IGBT	**3L-Hybrid-1**	**3L-Hybrid-2**	**2L-SiC**
Circuit Schematics				
T1/T2 and D1/D2	IKW40N120H3 *1200V 40A IGBT/FWD*	IMW120R045T1 *1200V 45mΩ CoolSiC™ MOS*	IMW120R045T1 *1200V 45mΩ CoolSiC™-MOS*	IMZ120R045T1 *1200V 45mΩ CoolSiC™-M*

						O S	
T3/T4	IKW30N65ES5 *650V 30A S5 IGBT*	IKW30N65ES5 *650V 30A S5 IGBT*		IKW30N65ES5 *650V 30A S5 IGBT*		-	
D3/D4	IKW30N65ES5 *650V 30A Rapid1 FRD*	IKW30N65ES5 *650V 30A Rapid1 FRD*		IDH16G65C5 *650V 16A Gen5 SBD*		-	
f_{sw} [kHz]	24	24	48	48	72	24	48
P_{max} [kW](1)	4	5	4.2	5.2	4.7	5.2	4.1
η_{max} [%] (2)	98.5	99	98.5	98.8	98.6	98.8	98.3

(1) P_{max} refers to the output power that can be reached before exceeding 100 °C device temperature measured at the package case front side; (2) η_{max} refers to the maximum efficiency value that is reached.

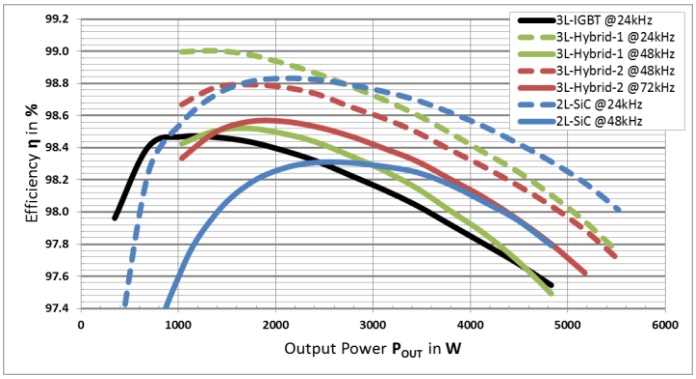


Figure 8: Measured efficiency comparison of the selected inverter solutions at cos(φ)=1.

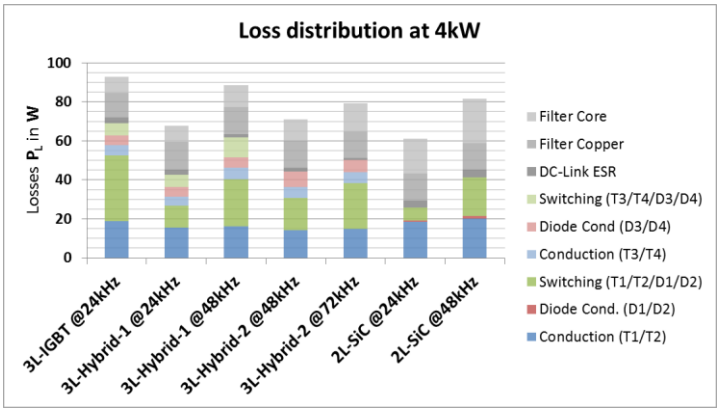


Figure 9: Estimated loss breakdown for the considered inverter solutions at cos(φ)=1.

IGBT three-level solution: *3L-IGBT*

As the three-level, pure silicon IGBT solution is commonly found in the industry, it serves as a benchmark within this work. As depicted in **Figure** 8 and Figure 9, 4 kW output power per phase and a peak efficiency of 98.5 % were reached at a switching frequency of 24 kHz. A slight increase of efficiency and output power could be achieved with a lower switching frequency, at the expenses of a larger filter to maintain the same ripple and EMI figures.

Hybrid three-level solution: *3L-Hybrid-1*

A more efficient way of reducing the switching losses and thus reaching a higher degree of freedom in the design is to replace the switches T1 and T2 of the NPC-1 Inverter by CoolSiC™ MOSFETs, leading to the solution referred to as *3L-Hybrid-1*. Depending on the design goal, either the output power can be increased by 25 % or the switching frequency can be doubled to reduce the output filter's size and cost.

Hybrid three-level solution: *3L-Hybrid-2*

A further performance improvement can be reached by replacing the Silicon Rapid 1 diodes D3/D4 with CoolSiC™ Schottky Barrier Diodes (SBD), leading to the third solution *3L-Hybrid-2*. In fact, at higher frequency operations, even a hyper-fast Silicon PN-junction diode like the Rapid 1 can limit the efficiency and the total output power. As it can be seen in Figure 9, the SiC diodes do increase the conduction losses of D3/D4 by some watts, but this is more than counterbalanced by the savings in switching losses of T1/T2 and D3/D4. Again, a designer can chose to optimize such a solution towards an increase of the output power or towards a higher switching frequency. Even tripling the frequency from 24 kHz to 72 kHz, an output power increase of 18 % is possible compared to the pure Silicon 3L-IGBT system. It should be considered that such a design is intended to mainly operate close to the unity power factor.

SiC MOSFET two-level solution: *2L-SiC*

Due to its high-speed nature, SiC switches can also give excellent performance in a two-level circuit. However, to maintain the same current ripple with a comparable inductor size, the switching frequency of a two-level solution needs to be roughly doubled compared to a three-level solution. At 48 kHz, the reference solution *2L-SiC* can reach a peak efficiency of 98.3 % and an output power of 4.1 kW. This is an important result especially when considering the increased core losses on the inductor. In fact the inductor is subject to suffer the same flux density swing at twice the frequency and to the higher voltage stress of the devices in a half bridge configuration. Although twice the voltage has to be switched at twice the frequency, the semiconductor losses are reduced by around 40 % compared to the *3L-IGBT* case. The reasons for this are not only the lower switching losses, but also the lower conduction losses given by the resistive characteristic of the MOSFET in forward and reverse direction. Synchronous rectification is required to bypass the high forward voltage drop of the CoolSiC™ MOSFET's body diode with the channel. In this operation, a small antiparallel SiC SBD dimensioned between 1/3 and 1/6 of the nominal current might be a good choice.

The suboptimal partial-load behavior of the two-level solution shown in the efficiency curves in **Figure** 8 can be explained by a high parasitic midpoint-capacitance, as a result of a suboptimal PCB layout. The influence of this capacitance on the switching losses can be roughly estimated by (eq.1)

(eq.1)

Due to the quadratic influence of the voltage and the linear impact of the frequency, a given midpoint capacitance has an eight times higher impact on the 48 kHz two-level solution than on the 24 kHz three-level solution.

Summary and outlook

Results presented in this document demonstrate that the use of SiC devices gives a relatively high degree of freedom in the design of a power electronic system. Depending on the specific design goal, higher output power levels and switching frequencies can be reached not only with pure SiC but also with hybrid SiC/Si solutions. Careful device selection is a key to replace Si components with SiC components only where it actually pays off.

It was also demonstrated, that existing three-level T-Type IGBT systems can be redesigned towards higher switching frequency and output power using SiC devices. It should be considered that the lower switching losses of a three-level solution come at the expense of higher circuit complexity.

Due to the unique device features, CoolSiC™ MOSFETs give extremely promising results in classical B6 inverters. Technically, such a solution is very elegant considering device utilization and the ability to handle full reactive power. Combined with the lower circuit complexity and thus higher reliability, it can be seen as an ideal candidate for bidirectional operation in applications not highly demanding in terms of EMI figures. However, with high speed, high voltage and high frequency switching, designing the output- and EMI-filter as well as the PCB becomes more challenging. In these areas, further practical research will be done in the future focusing on the comparative analysis of the present results versus the NPC-1 topology.