Low Coupling Capacitance SiC Full Bridge Inverter

Description of the power system

To provide accurate response to the important questions risen by designers two power systems were designed, respectively in three-level and in two-level topologies.

Two-level inverter design

The design of the two-level inverter was also completed within the cooperation between Infineon Technologies Austria A.G. and T.F. S.r.l. This system was designed to meet the CoolSiC™ MOSFET requirements, despite using standard PCB material and classical passive components. In this case, special care was dedicated to the dv/dt immunity and insulation levels to reach the highest possible dv/dt without negative impact on the reliability and on the system's stability. Further details of the power stage designed are represented in Figure 1 and indicated in Table 1. The block diagram is reported in Figure 2.

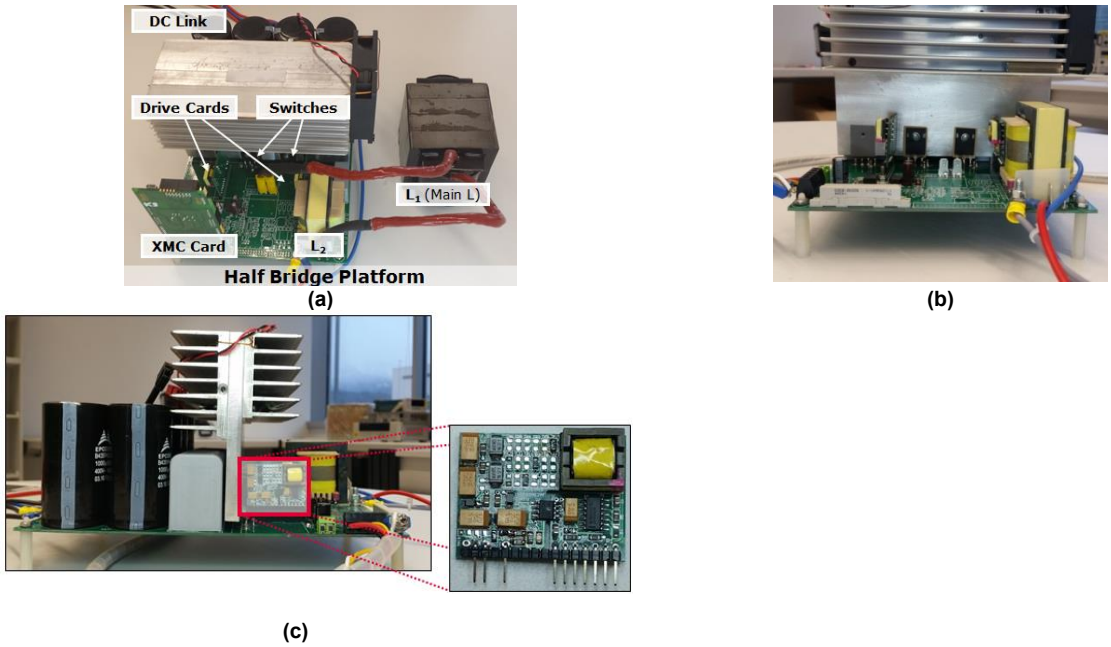

Figure 1: (a) close up view of a single-phase unit with short description of the main subsystems, (b) front view of the single-phase unit, (c) side view of the single-phase unit with a close-up view of a gate driver daughter board.

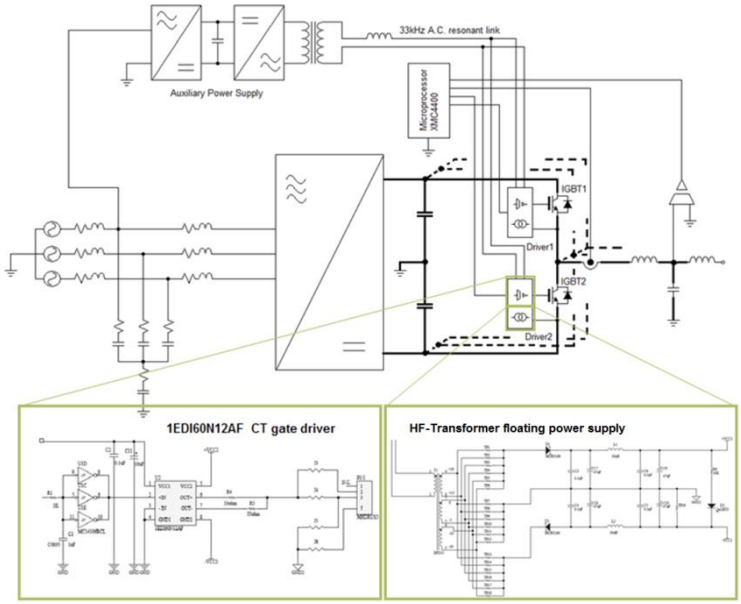

Figure 2: Block diagram of the two-level inverter system, sketched for a single-phase. Details of the coreless transformer and HF isolation transformer are indicated in the highlighted rectangles.

Table 1: Main electrical characteristic of the two-level testing system

Characteristic	Value	Unit
Semiconductor packages	Discrete IGBT and CoolSiC™ MOSFET in TO-247-3 and in TO-247-4, 1 discrete device per switch, 6 in total (possibility for paralleling operation of 2 x TO-247-3 and 2 x TO-247-4 per switch)	
Semiconductor types	S5/H5 IGBT, CoolSiC™ MOSFET, SiC Gen5/Rapid diode	
Input DC Voltage	500…700	V_{DC}
Output AC Voltage	400 (230 in single phase)	V_{AC}
Output current	30	A_{RMS}
Nominal output power	18 (6 per phase)	kW
Maximum P_{out} per 10s	25	kW
Maximum output current	25	A_{RMS}
Max allowable dv/dt	50	kV/µs
Max allowable di/dt	5	kA/µs
Insulation voltage	5	kV_{AC}
L_σ	34	nH
$T_{c(max)}$	120	°C

L-C-L output filter

The architecture of the output filter was designed using a classical L_1-C_1-L_2 configuration, as illustrated in Figure 3. L_1 is the output filter, C_1 is the output voltage filter and L_2 is the output EMI part of the filter. L_1 was dimensioned to allow a total ripple of 2 A_{pk}. This results in an inductor of 1 mH ±10% featuring Fe-Si E-Cores. The inductor is Class H designed for switching frequencies up to 50 kHz and DC-currents of up to 30 A in continuous operation at 150 °C. Equivalent series resistance amounts to R_{ESR}=25 mΩ and parasitic capacitance achieved is C_p=280 pF. C_1 is a 3.3 µF 2 kV_{AC} film capacitor. L_2 is a 100 µH Fe-Si E-Core inductor.

Figure 3: L-C-L output and EMI filter (a) single-phase schematic and (b) three-phase configuration. (c) L_1 inductor